REMARKS/ARGUMENTS

Enclosed herewith is a Terminal Disclaimer to overcome the provisional non-statutory obviousness – type double patenting rejection of claims 1 and 8 over copending Application Number 2005/0097552. Accordingly, it is respectfully submitted that this rejection is overcome.

Pending claims 22-29 stand rejected under 35 U.S.C. § 112, second paragraph as alleging allegedly omitting essential structural cooperative relationships of elements. Applicant respectfully traverses the rejection, as nowhere does the specification indicate that the subject matter claimed in claim 22 is "disclosed to be essential to the invention," or "necessary to practice the invention." MPEP § 2172.01. Furthermore, claim 22 has been amended to recite that the claimed wireless interface is coupled to the processor pipeline via a bus. For these reasons it is respectfully that the 35 U.S.C. § 112 rejection to claims 22-29 is overcome.

Pending claims 1, 8 and 13 stand rejected as indefinite for use of the phrase "may". Applicant respectfully traverses the rejection, as claims 1, 8 and 13 have been amended to remove the objected to language and replace it with the term "potentially". This claim language is sufficiently definite, as it is not exemplary claim language, i.e., "examples and preferences". MPEP § 2173.05(d). Accordingly, it is respectfully submitted that these claims define the subject matter "with a reasonable degree of particularity and distinctness." MPEP § 2173.02. No further requirement exists. Accordingly, it is respectfully submitted that rejection of claims 1, 8 and 13 for an alleged lack of definiteness is overcome.

Pending claims 1, 8, 13, 17 and 22 stand rejected under 35 U.S.C. § 101, as allegedly being directed to non-statutory subject matter. Applicant respectfully disagrees. Claim 1 has been amended to recite the execution of one or more instructions of the second thread after a switch. Accordingly, a physical transformation and practical application exists and the rejection of claim 1 is overcome. For similar reasons amended claim 8 defines patentable subject matter, as it recites execution of at least one instruction of the second thread after a switch. For at least the same reason, the rejection of claim 13 is also overcome.

As to the §101 rejection of claims 17 and 22, Applicant first notes that the claims recite "a processor pipeline". Such a processor pipeline is clearly hardware. Furthermore, both claims recite a feedback loop, i.e., hardware. Still further, claims 17 and 22 have been amended to recite first and second pipeline stages (in claims 17) and an instruction decoder and an

instruction fetch unit (in claim 22). Such tangible hardware is clearly statutory subject matter. Accordingly, the rejection of these claims under §101 is overcome.

Pending claims 1-3, 8, 10, 11 and 17 stand rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 6,049,867 (Eickemeyer). Applicant respectfully traverses the rejection. As to claim 1, Eickemeyer nowhere teaches determining whether instruction execution potentially causes a long latency. Instead, Eickemeyer teaches that if a cache miss occurs, threads are switched. This is not a potential cause of a long latency, but rather an actual long latency. Nowhere does Eickemeyer teach or suggest that a determination be made as to whether an instruction potentially causes a long latency. For at least this reason, claim 1 and its dependent claims are patentable over Eickemeyer. Dependent claim 2 is further patentable as Eickemeyer nowhere teaches execution of at least one additional instruction in the first thread while preparing to switch to a second thread. In this regard, the Office Action simply refers to saving a thread's state or determining enabling of thread switching. Office Action, page 6. However, Eickemeyer nowhere teaches that such actions are instructions of the first thread. Instead, these are performed outside of the thread. E.g., Eickemeyer, Figure 3 (note that execution of thread i in block 86 is separate and independent of determining if thread switching is enabled or saving of thread i state in blocks 90 and 92). Dependent claim 3 is further patentable as Eickemeyer nowhere teaches a determination based on a stochastic analysis. As defined in Applicant's specification, a stochastic analysis is a statistical basis, i.e., a knowledge that a condition "may, but need not necessarily," cause a latency. Specification, page 8, lns. 12-16. The valid bit of Eickemeyer is not a statistical model. Accordingly, for this further reason claim 3 is patentable. For at least the respective same reasons, claims 8, 10 and 11 are also patentable over Eickemeyer.

Claim 17 is patentable over Eickemeyer, as Eickemeyer nowhere teaches a feedback loop coupled between first and second pipeline stages to provide a feedback signal from the second stage back to the first stage. In this regard, the Office Action merely refers to a flowchart of Eickemeyer that discloses passing control from a first thread to a second thread. However, nowhere does this method teach a feedback signal, nor a feedback loop coupled between multiple pipeline stages to provide the feedback signal between the stages. Accordingly, claim 17 is patentable over Eickemeyer.

Pending claims 1-6, 8-9, 11-14, and 16-21 stand rejected under §102(b) over U.S. Patent 6,076,157 (Borkenhagen). Applicant respectfully traverses the rejection. As to claim 1, Borkenhagen similarly nowhere teaches determining whether instruction execution potentially causes a long latency. Instead, Borkenhagen causes thread switches bases on actual inability execute an instruction of a thread. Borkenhagen, column 16, lines 38-51. This actual failure to execute is not a potential cause of a long latency. Accordingly, claim 1 and the claims depending therefrom are patentable over Borkenhagen. As to dependent claim 4, Borkenhagen further nowhere teaches that an instruction is applied to a lookup table that includes entries corresponding to predetermined conditions. Instead, the cited portions of Borkenhagen (Office Action, page 7) nowhere teach or suggest applying an instruction to a lookup table. Certainly, Borkenhagen nowhere further teaches or suggests providing a feedback signal if this instruction matches an entry in the lookup table, as recited by claim 5. For similar reasons described above regarding claim 1, the rejection of claims 8 and 13 over Borkenhagen is overcome, as Borkenhagen nowhere teaches thread switching if a condition that could potentially result in a stall occurs.

As to claim 17, the citation of a flowchart in Borkenhagen (Office Action, page 6) nowhere teaches the recited feedback loop coupled between multiple processor pipelines stages, as clearly this software executed flowchart does not teach or suggest such a hardware feedback loop. Accordingly, claim 17 and its dependent claims are patentable.

Claims 22 and 24-29 stand rejected under 35 U.S.C. § 103(a) over Borkenhagen in view of U.S. Patent Number 6,076,157 (Rompaey). This rejection is improper, at least for the failure of Borkenhagen to teach or suggest the claimed feedback loop coupled to provide a feedback signal from an instruction decoder to an instruction fetch unit. Nor does Rompaey remedy this failure.

The rejection is further improper as there is no basis to combine Borkenhagen with Rompaey. In this regard, Rompaey is directed to non-analogous art. MPEP § 2141.01. Instead of the multi-threaded processor of Borkenhagen, Rompaey is directed to co-design of hardware and software. The subject matter of Rompaey simply has no bearing on the claimed subject matter, or that of Borkenhagen. Rompaey describes in its background that:

> Digital communication techniques form the basis of the rapid breakthrough of modern consumer electronics, wireless and wired voice-and data networking products, broadband

networks and multi-media applications. Such products are based on digital communications systems, which are made possible by the combination of VLSI technology and digital signal processing.

Rompaey, col. 1, lns. 18-24.

This is the alleged motivation to combine Rompaey with the thread switching of Borkenhagen. Clearly, this portion (along with the rest of Rompaey) nowhere provides a motivation to combine its teaching with that of Borkenhagen. MPEP § 2143.01. Similarly, Borkenhagen fails to provide a motivation to combine its teaching with the hardware/software co-design of Rompaey. Accordingly, the proposed combination is improper and the rejection is overcome.

New dependent claim 30 is patentable at least for the same reasons as claim 4 from which it depends.

For at least the same reasons described above with regard to the independent claims, the various dependent claims rejected under § 103(a) over varying combinations are also patentable.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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